09/672517

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Richard K. Greicar

Attorney Docket No.: GENSP035

Patent: 6,920,543 B1

Issued: July 19, 2005

Title: METHOD AND APPARATUS FOR PERFORMING DISTRIBUTED PROCESSING OF PROGRAM CODE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on September 15, 2005 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

TITLE PAGE:

1. Please add the following U.S. Patent Documents in the "References Cited" section:

--3,949,376	4/1976	Ball et al	711/125
4,225,922	9/1980	Porter	711/123
4,442,448	4/1984	Hall	711/125
5,148,533	9/1992	Joyce et al	711/144
5,479,638	12/1995	Assar et al	711/103
5,491,827	2/1996	Holtey	711/163
5,634,108	5/1997	Freeman	711/118
6,202,143	3/2001	Rim	712/210--

This appears correctly in the Information Disclosure Statement as filed on February 24, 2004.

2. Please add the following U.S. Patent Documents in the "References Cited" section:

--Re. 34,850	2/1995	Murakami et al.	83/513
3,596,257	7/1971	Patel et al.	711/171
3,753,239	8/1973	Lindsey et al.	711/156
4,084,224	4/1978	Appell et al.	718/100
4,888,691	12/1989	George et al.	714/15
5,465,361	11/1995	Hoenninger III	717/168
5,499,348	3/1996	Araki et al.	712/207
5,765,025	6/1998	Morimoto et al.	710/23
5,968,143	10/1999	Chisholm et al.	710/23
6,058,474	5/2000	Baltz et al.	713/1
6,161,169	12/2000	Cheng	711/150
6,170,049	1/2001	So	712/35
6,182,203	1/2001	Simar, Jr. et al.	712/22--

This appears correctly in the Information Disclosure Statement as filed on December 29, 2003.

SPECIFICATION:

1. Column 3, line 43, change "External memory 10" to --External memory 110--.

This appears correctly in the patent application as filed on September 27, 2000, on page 4, line 22.

2. Column 3, line 49, change "Memory 116" to --Memory blocks 116--. This appears correctly in the patent application as filed on September 27, 2000, on page 4, line 26.

3. Column 6, line 43, change "topped off within" to --topped off with--. This appears correctly in the patent application as filed on September 27, 2000, on page 8, line 30.

CLAIMS:

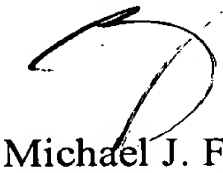
1. In line 20 of claim 1 (column 12, line 45) add --semaphore-- after "value". This appears correctly in the Amendment D as filed on October 18, 2004, on page 2, paragraph 1, line 15, as claim 20.

2. In line 6 of claim 4 (column 13, line 6) change "code or in" to --code or data in--. This appears correctly in the Amendment D as filed on October 18, 2004, on page 3, paragraph 2, line 4, as claim 23.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. GENSP035).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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650-961-8300

Form 1449 (Modified)	Atty Docket No.	Application No.:
Information Disclosure Statement By Applicant	GENSP035	09/672,517
	Applicant: Greicar	
	Filing Date	Group
(Use Several Sheets if Necessary)	September 27, 2000	2187

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	3,949,376	04/06/76	Ball et al.			
	B	4,225,922	09/30/80	Porter			
	C	4,442,488	04/10/84	Hall			
	D	5,148,533	09/15/92	Joyce et al.			
	E	5,479,638	12/26/95	Assar et al.			
	F	5,491,827	02/13/96	Holtey			
	G	5,561,786	10/01/96	Morse			
	H	5,634,108	05/27/97	Freeman			
	I	6,202,143	03/13/01	Rim			
	J						
	K						
	L						
	M						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	J							
	K							
	L							
	M							
	N							

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. GENSP035 Applicant: Greicar Filing Date September 27, 2000	Application No.: 09/672,517 Group 2187

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	Re. 34,850	02/07/95	Murakami et al.			
	B	3,596,257	07/27/71	Patel et al.			
	C	3,753,239	08/14/73	Lindsey et al.			
	D	4,084,224	04/11/78	Appell et al.			
	E	4,888,691	12/19/89	George et al.			
	F	5,465,361	11/07/95	Hoenninger, III			
	G	5,499,348	03/12/96	Araki et al.			
	H	5,765,025	06/09/98	Morimoto et al.			
	I	5,968,143	10/19/99	Chisholm et al.			
	J	6,058,474	05/02/00	Baltz et al.			
	K	6,161,169	12/12/00	Cheng			
	L	6,170,049	01/02/01	So			
	M	6,182,203	01/30/01	Simar, Jr. et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	J							
	K							
	L							
	M							
	N							

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. – 19. (canceled)

20. (currently amended) A method of ~~**distributed processing**~~ **storage and processing** by a processor, comprising:

providing a memory having a plurality of memory segments capable of storing either program code or data;

providing a storage location for capable of storing semaphore values each of which are associated with one of said memory segments and operable to indicate whether said associated memory segment contains program code or data that is available for use by the processor;

providing a first program and a second program each operable to access the semaphore values;

accessing a first semaphore value by said first program;

determining if the program code or data in the memory segment associated with the first semaphore value is available for use by the processor based upon the first ~~**semifore**~~ **semaphore** value; and

using the first program to implement the code or data stored in the memory segment associated with the first semaphore value by the processor**;**

wherein the program code or data stored in the memory segment associated with the first semaphore value represents one of a plurality of blocks of program code or data collectively representing an algorithm too large to be stored in the memory segment associated with the first semaphore value, thereby enabling execution of the algorithm using limited amount of memory.

21. (previously presented) A method as recited in claim 20, comprising:

altering the first semaphore value by the first program so as to indicate that the memory segment associated with the first semaphore value is available for having program code or data stored therein.

22. (previously presented) A method as recited in claim 21, comprising:

accessing the altered first semaphore value by the second program;

determining if the memory segment associated with the altered first semaphore value is available to have program code or data stored therein by the second program; and

using the second program to store code or data in the memory segment associated with the semaphore value when the associated memory segment is available.

23. (previously presented) A method as recited in claim 22, comprising:

completing the storing of the program code or data in the memory segment associated with the semaphore value by the second program; and

altering the semaphore value by the second program to indicate that the program code or data in the memory segment associated with the first semaphore value is available for use by the first program.

24. (previously presented) A method as recited in claim 20, wherein the memory is a local memory of the processor and wherein the memory segments are logical memory segments implemented by the processor based upon a computer program to be executed by the processor.

25. (previously presented) A method as recited in claim 20 wherein the storage location is a register, or portions thereof, of the processor or a scalar accessible to the processor.

26. (previously presented) A method as recited in claim 20, wherein the first program is a routine that is located in a reserved portion of the local memory such that the first program can not be written over with previously presented code or data, and wherein the first program is operable to access the code or data stored in the local memory of the processor as well as implement that accessed code or data.

27. (previously presented) A method as recited in claim 26, wherein when the program that is operable to implement a portion of a Fast Fourier Transform (FFT) program is stored in the local memory, the first program is operable to access the local memory and begin implementing the FFT code.

28. (previously presented) A method as recited in claim 27, wherein the second program is operable to load previously presented blocks of code or data that are used by the first program.

remaining half is reserved so that the support code for the invention can be stored there. Similarly, local memory block 108 is preferably approximately 8 kilobytes in size. Three kilobytes of the local memory block 108 are held in reserve for the invention's variable storage while 5 kilobytes are used to store data. The portions of memory blocks 106 and 108 that are used for code and data respectively are partitioned or segmented into units. Hence, local memory block 106 is considered to have 4 "slots" or units of memory of 1 kilobyte in size. Similarly, local memory block 108 is considered to have 5 "slots" or units of memory of 1 kilobyte in size. Note that the invention can operate with different slot counts and sizes; hence block 106 could have 8 blocks of size 512 bytes. The local memory blocks 106 and 108 are accessible by the CPU 104 of the processor via a bus (not shown). A register 150, designated as "R31" is shown as part of CPU 104. Such a register can be utilized to store a flag or "semaphore." Individual bit locations of the register can be associated with the code and data segments in local memory 106 and 108. In this way, different routines keep track of whether a segment of local memory is occupied, being loaded, available for loading new code or data, etc. In addition, CPU registers, such as R31, can be accessed more rapidly than RAM variables.

Figure 1 also shows an external memory 110, i.e., memory separate from the processor. External memory 110 is preferably synchronized dynamic random access memory (SDRAM) coupled to processor 102. However, it is envisioned that this external memory could take the form of other memory devices as well. Furthermore, while the memory is shown as being located within electronic device 100, in some embodiments it might be preferable to locate it external from such a device. External memory 110 is shown storing code for several algorithms. Namely, a Discrete Cosine Transform (DCT) algorithm is shown stored in a memory block 112 as divided into 4 segments of code, DCT1, DCT2, DCT3, and DCT4. Similarly, an AC-3 routine is shown stored in memory block 114 as code segments AC-3 #1, AC-3 #2, AC-3 #3, and AC-3 #4. Memory blocks 116 and 118 are shown storing code for Fast Fourier Transform (FFT) and an Echo special effects algorithm, respectively. For example, while the code stored in memory 112 would normally be considered just a DCT routine, it is segmented into four segments or blocks so that each block can fit into the limited memory capacity of processor 102, namely into the available slots of local memory 106 and 108 depending on whether code or data is being transferred, respectively.

Figures 2A and 2B show a flow chart 200 that demonstrates a method for implementing an embodiment of the invention. In Figure 2, a processor is provided with

2. All frames in a stream have essentially the same length and produce the same number of samples when decoded. This produces a direct relationship between data size and audio duration.

Because of this, an Audio Decoder at the highest level is just an initialization routine followed by a loop that decodes frames one at a time. Because the invention supports optional plugins, the act of decoding a single frame can be a little more complex:

1. The audio decoder converts one compressed frame into M channels of PCM data consisting of N 32-bit samples.

2. An optional plug-in takes the M channels of N samples and reprocesses them into K channels of N 32-bit samples. In other words, a plug-in can modify the original samples and might reorganize them into new channels, too.

3. After the decoded samples are prepared for output, the audio decoder can process the next frame by looping back to step 1.

Audio decoders and plug-ins execute entirely in the processor. While they can save and retrieve data in external memory, they cannot modify it outside of the processor. Inside the processor, Audio Decoders and Plug-ins only have about 4.5K of instruction memory and 5.5K of data memory. This makes it advisable to partition the code and data of an Audio Decoder or Plug-in into smaller stand-alone units called overlays.

To show how algorithm partitioning translates into overlays, this example will be presented based loosely on AC-3. Functionally, this Audio Decoder breaks down to the following stages:

1. Initialize
2. Find beginning of next frame
3. Build exponent tables from input (six channels)
4. Build mantissa tables from input (six channels)
5. For each of the six channels: do a Discrete Cosine Transform (DCT), followed by a Fast Fourier Transform (FFT), followed by another DCT and topped off with a Downmix of the six channels to two
6. Apply any additional algorithms (e.g., Karaoke)
7. Output the final downmixed channels
8. If there is more data to decode, go to step 2.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,920,543 B1

DATED : July 19, 2005

INVENTOR(S) : Richard K. Greicar

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Title Page:

Please add the following U.S. Patent Documents in the "References Cited" section:

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5,491,827	2/1996	Holtey..... 711/163
5,634,108	5/1997	Freeman..... 711/118
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4,888,691	12/1989	George et al..... 714/15
5,465,361	11/1995	Hoenninger III.....717/168
5,499,348	3/1996	Araki et al..... 712/207
5,765,025	6/1998	Morimoto et al..... 710/23
5,968,143	10/1999	Chisholm et al..... 710/23
6,058,474	5/2000	Baltz et al..... 713/1
6,161,169	12/2000	Cheng..... 711/150
6,170,049	1/2001	So..... 712/35
6,182,203	1/2001	Simar, Jr. et al..... 712/22--

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UNITED STATES PATENT AND TRADEMARK OFFICE
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PATENT NO. : 6,920,543 B1

DATED : July 19, 2005

INVENTOR(S) : Richard K. Greicar

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Specification:

Column 3, line 43, change "External memory 10" to --External memory 110--.

Column 3, line 49, change "Memory 116" to --Memory blocks 116--.

Column 6, line 43, change "topped off within" to --topped off with--.

Claims:

In line 20 of claim 1 (column 12, line 45) add --semaphore-- after "value".

In line 6 of claim 4 (column 13, line 6) change "code or in" to --code or data in--.

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